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Agilent Technologies

The HP 1660C/CS/CP-Series Benchtop Logic Analyzers

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Technical Data

Identifying the cause of problems in embedded microprocessor system designs can be difficult. The HP 1660C/CS/CP-series benchtop logic analyzers have the features to help the design team troubleshoot hardware and find software defects quickly. Team members can verify critical hardware timing relationships, view processor mnemonics, make analog parametric measurements, or functionally test their digital design with stimulus.

An optional LAN interface enables software designers to capture a real-time microprocessor trace and time-correlate it to source code in C++ or other high-level languages on a PC or workstation. For time-correlation of source code, order the HP B3740A Software Analysis package.

The combination of 100-MHz state, 500-MHz timing, 2-channel 250-MHz BW scope, or 32-channel 200 M Vector/sec pattern generator, internal hard disk drive, and LAN make the HP 1660C/CS/CP-series benchtop logic analyzers especially well suited to finding problems at the integration stage of prototype hardware and software. [1]

- The internal hard disk drive provides quick storage and retrieval of files.[1]
- 3.5-inch high-density flexible disk drive supports both DOS and LIF formats.
- LAN interface enables access to the logic analyzer files via FTP or NFS. Use X11 windows and display the logic analyzer user interface on a PC or workstation. [1]
- The HP 1660C/CS/CP-series operating system includes System Performance Analysis (SPA). SPA provides state histograms, state overview, and time interval analysis.
- The HP E2450A Symbolic Download Utility is included with the HP 1660C/CS/CP-series. This utility provides the capability to extract symbolic information from popular object module formats.
- Store data as ASCII files and screen images in TIFF, PCX, and EPS (encapsulated PostScript™) formats.
- New graphical trigger macros make trigger setup easier.
- Centronics, RS-232 and HP-IB communications ports make connecting to other devices easier than ever. All of these come standard on all HP 1660C/CS/CP-series models.
- Standard DIN mouse and keyboard connectors. A mouse ships with every HP 1660C/CS/CP-series.[1]

Get to the root cause of problems quickly.

[1] Please refer to HP 1664A Product Specifications and Characteristics on page 9.

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Logic Analyzer Key Specifications and Characteristics

HP Model Number	1660C/CS/CP	1661C/CS/CP	1662C/CS/CP	1663C/CS/CP	1664A
State and Timing Channels	136	102	68	34	34
Timing Analysis	Conventional: 250 MHz all channels, 500 MHz half channels Transitional: 125 MHz all channels, 250 MHz half channels Glitch: 125 MHz half channels				
State Analysis Speed	100 MHz, all channels				50 MHz
State Clocks/Qualifiers	6	6	4	2	2
Memory Depth per Channel	4K per channel, 8K in half-channel modes				
LAN Port	Standard for CP Model, Option 015 for C/CS model				N/A

Pattern Generator Key Specifications and Characteristics

HP Model Number	1660CP, 1661CP, 1662CP, 1663CP		
Maximum Clock Speed	200 MHz	100 MHz	50 MHz
Number of Data Channels	16	32	32
Memory Depth, in vectors	258,048	258,048	258,048
"IF" Command	No	No	Yes

Oscilloscope Key Specifications and Characteristics

Model Number	HP 1660CS, HP 1661CS, HP 1662CS & HP 1663CS
Channels	2
Maximum Sample Rate	1 GSa/s per channel
Bandwidth	dc to 250 MHz (dc coupled)
Rise Time	1.4 ns
Vertical Resolution	8 bits
Memory Depth per Channel	8k samples

HP 1660C/CS/CP-Series General-Product Information

Human Interface

Front Panel A knob and keypads make up the front-panel human interface. Keys include control, menu, display navigation, and alpha-numeric entry functions.

Mouse A DIN mouse is shipped as standard equipment. It provides full instrument control. Knob functionality is replicated by holding down the right button and moving the mouse left or right. [1]

Keyboard The logic analyzer can also be operated using a DIN keyboard. Order the HP Logic Analyzer Keyboard Kit, model number HP E2427B. [1]

Input/Output, Control, and Printing

I/O Ports All units ship with a Centronics parallel printer port, RS-232, and HP-IB as standard equipment.[1]

LAN Interface An Ethernet LAN interface is available as option 015. The LAN interface comes with both Ethertwist and ThinLan connectors. The LAN supports FTP and PC/NFS connection protocols. It also works with X11 windows packages. [1][2]

Programmability Each instrument is fully programmable from a computer via HP-IB and RS-232 connections. This feature is standard on all models.

HP Printer Support Printers which use the HP Printer Control Language (PCL) and have a parallel Centronics, RS-232 or HP-IB interface are supported:
HP DeskJet, LaserJet, QuietJet, PaintJet, and ThinkJet models

Alternate Printer Supported The Epson FX80, LX80 and MX80 printers with an RS-232 or Centronics interface are supported in the Epson 8-bit graphics mode.

Hard Copy Output Screen images can be printed in black and white from all menus using the *Print* field. State or timing listings can be also be printed in full or part (starting from center screen) using the *Print All* selection.

Mass Storage Files and Software

Updating the Operating System The operating system resides in Flash ROM and can be updated from the flexible disk drive or from the internal hard disk drive. The HP 1664A boots from disk and requires only a disk change to update the operating system.

Mass Storage Supported by an internal hard disk drive and by a 1.44 Mbyte, 3.5-inch flexible disk drive. Supports DOS and LIF formats. [1]

Screen Image Files An image file of any display screen can be stored to disk via the display's *Print* field. Black & white TIFF, Grayscale TIFF, PCX, Encapsulated PostScript™ (EPS), and gray-scale TIFF file formats are available.

ASCII Data Files State or timing listings can be stored as ASCII files on a disk via the display's *Print* field. These files are equivalent in character width and line length to hard-copy listings printed via the *Print All* selection.

Configuration and Data Files Logic analyzer and oscilloscope files that include configuration and data information (if present) are encoded in a binary format. They can be stored to or loaded from the hard disk drive or a flexible disk. [1]

Recording of Acquisition and Storage Times Binary format configuration/data files are stored with the time of acquisition and the time of storage for all models except the HP 1664A, which does not have a real-time clock.

Acquisition Arming

Initiation Arming is started by *Run, Group Run,* or the Port In BNC.

Cross Arming Analyzer machines and the oscilloscope can cross-arm each other. [1]

Output An output signal is provided at the Port Out BNC.

Port In/Out

PORT IN Signal and Connection Port In is a standard BNC connection. The input operates at TTL logic signal levels. Rising edges are valid input signals.

PORT OUT Signal and Connection Port Out is a standard BNC connection with TTL logic signal levels. A rising edge is asserted as a valid output.

Skew Adjustment and Arming Times

Skew Adjustment Correction factors for nominal skew between displayed timing and oscilloscope signals are built into the operating system. Additional correction for unit-by-unit variation can be made using the *Skew* field. An entered skew value affects the next (not the present) acquisition display.

[1] Please refer to HP 1664A Product Specifications and Characteristics on page 9.

[2] LAN interface is standard for the HP 1660CP-series, optional for the HP 1660C/CS-series.

HP 1660C/CS/CP-Series Logic Analyzer Specifications and Characteristics

PORT IN Arms Logic Analyzer [3]	15 ns typical delay from signal input to a *don't care* logic analyzer trigger.
PORT IN Arms Oscilloscope	40 ns typical delay from signal input to an *immediate* oscilloscope trigger; not available when oscilloscope is in time-qualified pattern triggering mode.
Logic Analyzer Arms PORT OUT [3]	120 ns typical delay from logic analyzer trigger to signal output.
Oscilloscope Arms PORT OUT	60 ns typical delay from oscilloscope trigger to signal output.

Operating Environment

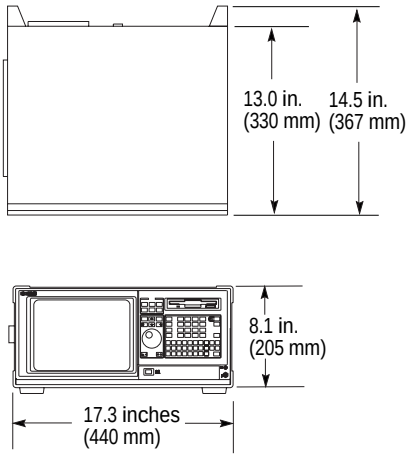
Power	115 Vac or 230 Vac, –22% to +10%, single phase, 48-66 Hz, 320 VA max
Temperature	Instrument, 0° to 50° C (+32° to 122° F). Disk media, 10° to 40° C (+50° to 104°F). Probes and cables, 0° to 65° C (+32° to 149° F)
Humidity	Instrument, up to 95%, relative humidity at +40° C (+140° F). Disk media and hard drive, 8% to 85% relative humidity.
Altitude	To 3,048 m (10,000 ft) [1]
Vibration: Operating	Random vibrations 5–500 Hz, 10 minute per axis, ~ 0.3 g (rms).
Vibration: Non Operating	Random vibrations 5–500 Hz,10 minutes per axis,~ 2.41 g (rms); and swept sine resonant search, 5–500 Hz, 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

Physical Factors

Weight	28.6 lbs. (13 kg) [1]
Dimensions	See figure 1
Safety	IEC 348/ HD 401, UL 1244, and CSA Standard C22.2 No. 231 (series M-89)

EMC

CISPR 11:1990/EN 55011 (1991): Group 1 Class A
IEC 801-2:1991/EN 50082-1 (1992): 4kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m
IEC 801-4:1988/EN 50082-1 (1992): 1kV

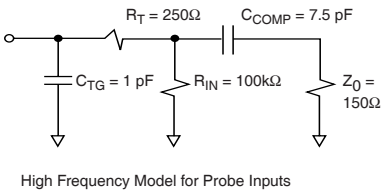


Weight 28.6 lbs (13 kg)

Figure 1

Logic Analyzer Probes

Input Resistance	100 kΩ ±2%
Input Capacitance	approx. 8 pF (see figure 2)



High Frequency Model for Probe Inputs

Figure 2

Minimum Input Voltage Swing	500 mV peak-to-peak
Minimum Input Overdrive	250 mV or 30% of input amplitude, whichever is greater
Threshold Range	–6.0 V to +6.0 V in 50-mV increments
Threshold Setting	Threshold levels may be defined for pods (17-channel groups) on an individual basis
Threshold Accuracy*	± (100 mV +3% of threshold setting)
Input Dynamic Range	± 10 V about the threshold
Maximum Input Voltage	± 40 V peak
+5 V Accessory Current	1/3 amp maximum per pod
Channel Assignment	Each group of 34 channels (a pod pair) can be assigned to Analyzer 1, Analyzer 2 or remain unassigned.

[1] Please refer to HP 1664A product specifications and characteristics on page 9.

[3] Time may vary depending upon the mode of logic analyzer operation.

* Warranted specification.

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State Analysis

Maximum State Speed*	100 MHz all models except HP 1664A, which is 50 MHz
Channel Count [4]	HP 1660C, CS, CP 136/68 HP 1661C, CS, CP 102/51 HP 1662C, CS, CP 68/34 HP 1663C, CS, CP 34/17 HP 1664A 34/17
Memory Depth per Channel [4]	4096/8192 samples

State Clocks

HP 1660C, CS, CP	6 clocks
HP 1661C, CS, CP	6 clocks
HP 1662C, CS, CP	4 clocks
HP 1663C, CS, CP	2 clocks
HP 1664A	2 clocks

Clocks can be used by either one or two state analyzers at any time, except for the 1663C, 1663CS, 1663CP and 1664A models, which can have only one state or timing analyzer. Clock edges can be ORed together and operate in single phase, two-phase demultiplexing, or two-phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.

State Clock Qualifier	The high or low of up to 4 of the 6 clocks can be ANDed or ORed with the clock specification.

Setup/Hold* [5]

one clock, one edge	3.5/0 ns to 0/3.5 ns (in 0.5 ns increments)
one clock, both edges	4.0/0 ns to 0/4.0 ns (in 0.5 ns increments)
multi-clock, multi-edge	4.5/0 ns to 0/4.5 ns (in 0.5 ns increments)

Minimum State Clock Pulse Width* [5]	3.5 ns
Minimum Master to Master Clock Time* [5]	10.0 ns
Minimum Slave to Slave Clock Time [5]	10.0 ns
Minimum Master to Slave Clock Time [5]	0.0 ns
Minimum Slave to Master Clock Time [5]	4.0 ns
Clock Qualifiers Setup/Hold [5]	4.0/0 ns (fixed)
State Tagging [6]	Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Max. count is 4.29×10^9.
State Tag Count	0 to 4.29×10^9
State Tag Resolution	1 count
Time Tagging [6]	Measures the time between stored states, relative to either the previous state or to the trigger. Max. time between states is 34.4 sec. Min. time between states is 8 ns.
Time Tag Value	8 ns to 34.4 seconds ± (8 ns + 0.01% of time tag value)
Time Tag Resolution	8 ns or 0.1% (whichever is greater)

Timing Analysis

Conventional Timing	Data stored at selected sample rate across all timing channels.
Maximum Timing Speed [4]	250 MHz / 500 MHz
Channel Count [4]	HP 1660C, CS, CP 136/68 HP 1661C, CS, CP 102/51 HP 1662C, CS, CP 68/34 HP 1663C, CS, CP 34/17 HP 1664A 34/17
Sample Period [4]	4 ns/2 ns minimum, 8.38 ms maximum
Memory Depth per Channel [4]	4096/8192 samples
Time Covered by Data	Sample period × memory depth 16.3 µs min, 34.4 sec/68.6 sec max
Transitional Timing	Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.
Maximum Timing Speed [4]	125 MHz/250 MHz
Channel Count [4]	HP 1660C, CS, CP, 136/68 HP 1661C, CS, CP 102/51 HP 1662C, CS, CP 68/34 HP 1663C, CS, CP 34/17 HP 1664A 34/17
Sample Period [4]	8 ns/4 ns
Time Covered by Data [4]	16.3 µs minimum, 9.7 hrs./6.5 hrs. maximum
Maximum Time Between Transitions	34.4 s
Number of Captured Transitions [4]	1023-2047/682-4094 Depending on input signals

[4] Full Channel /Half Channel Modes

[5] Specified for an input signal VH= – 0.9V, VL = – 1.7V, slew rate = 1V/ns, and threshold = –1.3V

[6] Time or-state-tagging (Count Time or Count State) is available in the full-channel state mode. There is no speed penalty for tag use. Memory is halved when time or state tags are used unless a pod pair (34-channel group) remains unassigned in the Configuration menu.

* Warranted specification.

Glitch Capture Mode	Data sample and glitch information is stored every sample period
Maximum Timing Speed	125 MHz
Channel Count	HP 1660C ,CS, CP 68 HP 1661C, CS, CP 51 HP 1662C, CS, CP 34 HP 1663C, CS, CP 17 HP 1664A 17
Sample Period	8 ns minimum, 8.38 ms maximum
Minimum Glitch Width*	3.5 ns
Maximum Glitch Width	Sample Period – 1 ns
Memory Depth per Channel	2048 samples
Time Covered by Data	Sample Period × 2048: 16.3 µs minimum, 17.1 sec maximum

Time Interval Accuracy

Sample Period Accuracy	± 0.01%
Channel-to-Channel Skew	2 ns typical, 3 ns maximum
Time Interval Accuracy	± (Sample Period Accuracy + channel-to-channel skew + 0.01% of time interval reading)
Maximum Delay After Triggering	Sample Period 2-8 ns : 8.389 ms Sample Period > 8 ns: 1,048,575 × sample period

Trigger Specifications

Trigger Macros	Trigger setups can be selected from a categorized list of trigger macros. Each macro is shown in graphical form and has a written description. Macros can be chained together to create a custom trigger sequence.
Pattern Recognizers	Each recognizer is the AND combination of bit (0,1, or X) patterns in each label.
Pattern Recognizers	10
Pattern Width (in channels)[4]	HP 1660C, CS, CP 136/68 HP 1661C, CS, CP 102/51 HP 1662C, CS, CP 68/34 HP 1663C, CS, CP 34/17 HP 1664A 34/17
Minimum Pattern and Range Recognizer Pulse Width	250 MHz and 500 MHz Timing Modes: 13 ns + channel-to-channel skew ≤ 125 MHz Timing Modes : 1 sample period + 1 ns + channel-to-channel skew + 0.01%
Range Recognizers	Recognize data which is numerically between or on two specified patterns (ANDed combination of zeros and/or ones).
Range Recognizers	2
Range Width	32 channels
Edge/Glitch Recognizers	Trigger on glitch or edge on any channel. Edge can be specified as rising, falling or either.
Edge/Glitch Recognizers	2 (in timing mode only)
Edge/Glitch Width (in channels) [4]	HP 1660C, CS, CP 136/68 HP 1661C, CS, CP 102/51 HP 1662C, CS, CP 68/34 HP 1663C, CS, CP 34/17 HP 1664A 34/17
Edge/Glitch Recovery Time	Sample Period 2-8 ns: 28 ns Sample Period > 8 ns: 20 ns + sample period
Greater than Duration (timing only)	Sample period 2-8 ns: 8 ns to 8.389 ms. Accuracy is –2 ns to +10 ns Sample period > 8 ns: (1 to 2^{20}) × sample period. Accuracy is –2 ns + sample period + 2 ns ± 0.01%
Less than Duration (timing only)	Sample period 2-8 ns: 8 ns to 8.389 ms. Accuracy is –2 ns to +10 ns. Sample period > 8 ns: (1 to 2^{20}) × sample period. Accuracy is 2 ns + sample period – 2 ns ± 0.01%
Qualifier	A user-specified term that can be any state, no state, any recognizer, (pattern, ranges or edge/glitch), any timer, or the logical combination (NOT, AND, NAND, OR, NOR, XOR, NXOR) of the recognizers and timers.
Branching	Each sequence level has a branching qualifier. When satisfied, the analyzer will branch to the sequence level specified.

[4] Full Channel /Half Channel Modes

* Warranted specification

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Occurrence Counters	Sequence qualifier may be specified to occur up to 1,048,575 times before advancing to the next level. Each sequence level has its own counter.
Maximum Occurrence Count	1,048,575
Storage Qualification (state only)	Each sequence level has a storage qualifier that specifies the states that are to be stored.
Maximum Sequencer Speed	125 MHz
State Sequence Levels	12
Timing Sequence Levels	10
Timers	Timers may be Started, Paused, or Continued at entry into any sequence level after the first.
Timers	2
Timer Range	400 ns to 500 seconds
Timer Resolution	16 ns or 0.1% whichever is greater
Timer Accuracy	± 32 ns or ± 0.1%, whichever is greater
Timer Recovery Time	70 ns
Data In to Trigger Out BNC Port	110 ns typical

Acquisition, Measurement and Display Functions

Arming	Each analyzer can be armed by the Run key, the other analyzer, the oscilloscope (CS models only), the pattern generator (CP Models only) or the Port In. [1]
Run	Starts acquisition of data in specified trace mode.
Stop	In single trace mode or the first run of a repetitive acquisition, Stop halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, Stop halts acquisition of data and does not change current display.
Trace Mode	Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until Stop is pressed or until pattern time interval or compare stop criteria are met.
Trigger	Displayed as a vertical dashed line in the timing waveform, state waveform and X-Y chart displays and as line 0 in the state listing and state compare displays.
Activity Indicators	Provided in the Configuration, State Format, and Timing Format menus for monitoring device-under-test activity while setting up the analyzer.
Labels	Channels may be grouped together and given a 6-character name called a *label*. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label. Trigger terms may be given an 8-character name.

Measurement Functions

Markers	Two markers (x and o) are shown as dashed lines in the display.
Time Intervals	The x and o markers measure the time interval between events occurring on one or more waveforms or states (available in state when time tagging is on).
Delta States	The x and o markers measure the number of tagged states between any two states (state only).
Patterns	The x or o marker can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The o marker can also find the nth occurrence of a pattern before or after the x marker.
Statistics	x to o marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum x to o time, maximum x to o time, average x to o time, and ratio of valid runs to total runs.

1] Please refer to HP 1664A Product Specifications and Characteristics on page 9.

Compare Mode Functions	Performs post-processing bit-by-bit comparison of the acquired state data and Compare Image data.
Compare Image	Created by copying a state acquisition into the compare image buffer. Allows editing of any bit in the Compare Image to a 1, X or O.
Compare Image Boundaries	Each channel (column) in the Compare Image can be enabled or disabled via bit masks in the Compare Image. Upper and lower ranges of states (rows) in the compare image can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.
Stop Measurement	Repetitive acquisitions may be halted when the comparison between the current state acquisition and the current Compare Image is equal or not equal.
Compare Mode Displays	Reference Listing display shows the Compare Image and bit masks; Difference Listing display highlights differences between the current state acquisition and the Compare Image.

Data Entry/Display

Display Modes	State Listing, State Waveforms, State Chart, State Compare Listing, Compare Difference Listing, Timing Waveforms, Timing Listing, interleaved time-correlated listing of two state analyzers (time tags on), and time-correlated State Listing with Timing Waveforms on the same display.
State X-Y Chart Display	Plots value of a specified label (on y-axis) versus states or another label (on x-axis). Both axes can be scaled.
Markers	Correlated to State Listing, State Compare, and State Waveform displays. Available as pattern, time, or statistics (with time counting) and states (with state counting on).
Accumulate	Chart display is not erased between successive acquisitions.
State Waveform Display	Displays state acquisitions in waveform format.
States/div.	1 to 1000 states.
Delay	– 8191 to + 8192 states.
Accumulate	Waveform display is not erased between successive acquisitions.
Overlay Mode	Multiple channels can be displayed on one waveform display line.
Displayed Waveforms	24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.
Timing Waveform Display	Displays timing acquisition in waveform format.
Sec/div	1 ns to 1000 s; 0.01% resolution.
Delay	– 2,500 s to + 2,500 s
Accumulate	Waveform display is not erased between successive acquisitions.
Overlay Mode	Multiple channels can be displayed on one waveform display line. When waveform size set to large, the value represented by each waveform is displayed inside the waveform in the selected base.
Displayed Waveforms	24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.
System Performance Analysis	SPA includes state histogram, state overview and time interval measurements to aid in the software optimization process. These tools provide a statistical overview of your synchronous design.
Bases	Binary, Octal, Decimal, Hexadecimal, ASCII (display only), User-defined symbols, two's complement.
Symbols	
Pattern Symbols	User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs.
Range Symbols	User can define a mnemonic covering a range of values. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.
Number of Symbols	1000 maximum.

HP 1660CS-Series Oscilloscope Specifications and Characteristics [1]

General Information

Model Numbers	HP 1660CS, 1661CS, 1662CS, 1663CS
Number of Channels	2
Maximum Sample Rate	1 GSa/s per channel
Bandwidth [7] [11]	dc to 250 MHz (real time, dc coupled)
Rise Time [8] [11]	1.4 ns
Vertical Resolution	8 bits
Memory Depth	8k samples

Oscilloscope Probing

Input Coupling	1 MΩ: ac,dc 50 Ω: dc only
Input R [11]	1MΩ ± 1% 50Ω ± 1%
Input C	~ 7pF
Probes Included	Two HP 10430A probes; 10:1, 1 MΩ 6.5 pF

Vertical (at BNC)

Maximum Safe Input Voltage	1 MΩ : ±250 V 50 Ω : 5 V rms
Vertical Sensitivity Range (1:1 Probe)	1 MΩ: ±250 V (ac + dc, <10 kHz) 50 Ω: 5 V rms
Probe Factors	Any integer ratio from 1:1 to 1000:1
Vertical (dc) Gain Accuracy [9]	± 1.25% of full scale
dc Offset Range (1:1 probe)	± 2V to ± 250V (depending on the vertical sensitivity)
dc Offset Accuracy [11]	± [1.0% of channel offset + 2.0% of full scale]
Voltage Measurement Accuracy [11]	± [1.25% of full scale + offset accuracy + 0.016 V/div]
Channel-to-Channel Isolation	dc to 50 MHz – 40 dB 50 MHz to 250 MHz – 30 dB

Horizontal

Time Base Range	1 ns/div to 5 s/div
Time Base Resolution	20 ps ± [(0.005% of Δt) + (2 × 10⁻⁶ × delay setting) + 150 ps]
Maximum Negative Acquisition Delay	– 4 µs to – 40 s (depending on the sample rate)
Maximum Positive Acquisition Delay	16.7 ms to 2.5 ks (depending on sample rate)
Time Interval Measurement Accuracy [10] [11]	± [(0.005% of Δt) + (2×10⁻⁶ × delay setting) + 150 ps]

Oscilloscope Triggering

Trigger Level Range	Bounded within channel display window
Trigger Sensitivity [11]	dc to 50 MHz: 0.063 × Full Scale 50 MHz to 250 MHz: 0.125 × Full Scale

Trigger Modes

Immediate	Triggers immediately after arming condition is met. (Arming condition is Run, Group Run, cross arming signal, or Port In BNC signal).
Edge	Triggers on rising or falling edge from channel 1 or 2.
Pattern	Triggers on entering or exiting logical pattern specified across channels 1 or 2. Each channel can be specified as high (H), low (L), or don't care (X) with respect to the level settings in the edge trigger menu. Patterns must be >1.75 ns in duration to be recognized.
Time-Qualified Pattern	Triggers on the exiting edge of a pattern which meets the user-specified duration criterion. Greater than, less than, or within range duration criterion can be used. Duration range is 20 ns to 160 ns. Recovery time after valid patterns with invalid duration is <12 ns.
Events Delay	Triggers on the nth edge or pattern as specified by the user. Time-qualification is applied only to the 1st of n patterns.
Auto-Trigger	Self-triggers if no trigger condition is found ~ 50 ms after arming.

Measurement Functions

Time Markers	Two markers (x and o) measure time intervals manually, or automatically with statistics.
Voltage Markers	Two markers (a and b) measure voltage and voltage differences.
Automatic Measurements	Period, frequency, rise time, fall time, +width, –width, peak-to-peak voltage, overshoot, and undershoot.

[7] Upper bandwidth reduces by 2.5 MHz for every degree C above 35°C.

[8] Rise time calculated as $t_r = \frac{0.35}{\text{bandwidth}}$

[9] Vertical gain accuracy decreases 0.08% per degree C from software calibration temperature.

[10] Specification applies at the maximum sampling rate. At lower rates, replace 150 ps in the formula with (0.15 × sample interval) where sample interval is defined as 1/sample rate.

[11] Specifications (valid within ± 10°C of auto-calibration temperature)

HP 1660CP-Series Pattern Generator Characteristics

The HP 1664A Specifications and Characteristics

The HP 1664A is a low cost version of the HP 1660C/CS/CP-series logic analyzer family. The HP 1664A has some specifications and characteristics that are different from the HP 1660C/CS/CP-series logic analyzers.

The HP 1664A:

- Supports a maximum of 50 MHz state acquisition
- Supports all modes of timing analysis
- Weight 26 pounds (11.8 kg)
- Altitude To 15,000 ft (4,752 m)
- Boots from the floppy disk drive—it does not have flash ROM
- It cannot be upgraded to include an oscilloscope or pattern generator
- Channel count upgrades are not available
- The mouse and keyboard connectors are HP HIL standard
- For the optional keyboard order HP E2427A
- It cannot be upgraded to a C model
- It does not support the HP B3740A software analyzer software
- It does not support the HP E2450A Symbol Download Utility
- It does not support the software performance analysis software
- It does not have a hard disk drive
- It cannot have a LAN port added

Maximum memory depth	258,048 vectors
Number of output channels at 100 MHz to 200 MHz clock	16
Number of output channels at ≤100 MHz clock	32
Maximum number of "IF Condition" blocks at ≤50 MHz clock	1
Maximum number of different macros	100
Maximum number of lines in a macro	1024
Maximum number of parameters in a macro	10
Maximum number of macro invocations	1,000
Maximum loop count in a repeat loop	20,000
Maximum number of repeat loop invocations	1,000
Maximum number of Wait event patterns	4
Number of input lines to define a wait pattern	3
Maximum width of a label	32 bits
Maximum number of labels	126

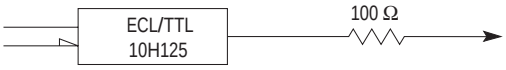
Lead Set Characteristics

HP 10474A 8-channel probe lead set	Provides most cost effective lead set for the HP 1660CP-series clock and data pods. Grabbers are not included.
HP 10347A 8-channel probe lead set	Provides 50 Ω coaxial lead set for unterminated signals, required for HP 10465A ECL Data Pod (unterminated). Grabbers are not included.

Data Pod Characteristics

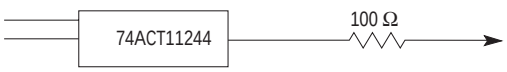
HP 10461A TTL DATA POD

Output type	10H125 with 100 Ω series
Maximum clock	200 MHz
Skew (note 1)	typical < 2 ns; worst case = 4 ns
Recommended lead set	HP 10474A



HP 10462A 3-STATE TTL/CMOS DATA POD

Output type	74ACT11244 with 100 Ω series; 10H125 on non 3-state channel 7 (note 2)
3-state enable	negative true, 100 KΩ to GND, enabled on no connect
Maximum clock	100 MHz
Skew (note 1)	typical < 4 ns; worst case = 12 ns
Recommended lead set	HP 10474A



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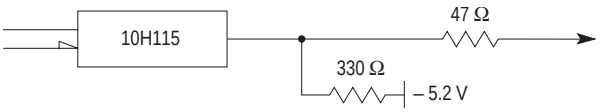
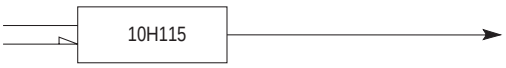
HP 10464A ECL DATA POD (TERMINATED)

Output type	10H115 with 330 Ω pulldown, 47 Ω series
Maximum clock	200 MHz
Skew (note 1)	typical < 1 ns; worst case = 2 ns
Recommended lead set	HP 10474A



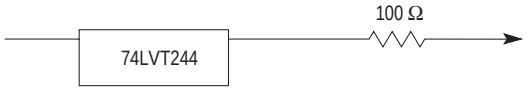
HP 10465A ECL DATA POD (UNTERMINATED)

Output type	10H115 (no termination)
Maximum clock	200 MHz
Skew (note 1)	typical < 1 ns; worst case = 2 ns
Recommended lead set	HP 10347A



HP 10466A 3-STATE TTL/3.3 VOLT DATA POD

Output type	74LVT244 with 100 Ω series; 10H125 on non 3-state channel 7 (note 2)
3-state enable	negative true, 100 KΩ to GND, enabled on no connect
Maximum clock	200 MHz
Skew (note 1)	typical < 3 ns; worst case = 7 ns
Recommended lead set	HP 10474A



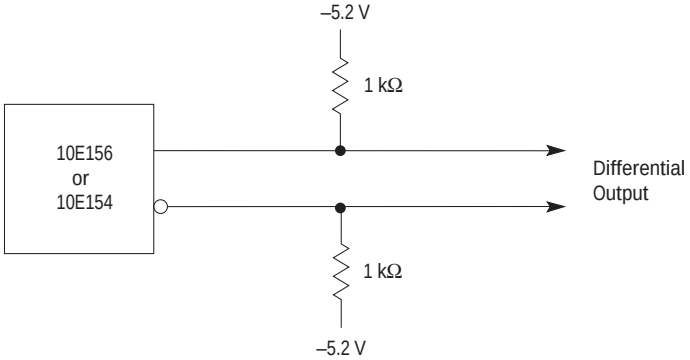
Note 1: Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within a single or multiple module system.

Note 2: Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

Data Cable Characteristics Without a Data Pod

The HP 1660CP data cables without a data pod provide an ECL terminated (1 KΩ to –5.2V) differential signal (from a type 10E156 or 10E154 driver). These are usable when received by a differential receiver, preferably with a 100 Ω termination across the lines. These signals should not be used single ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).

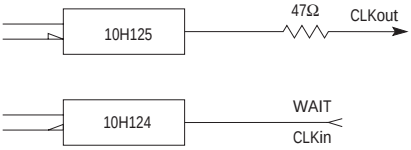
HP 1660CP DATA CABLE OUTPUT



Clock Pod Characteristics

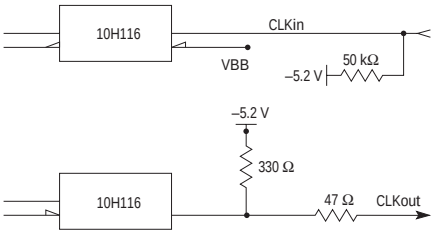
10460A TTL CLOCK POD

Clock output type	10H125 with 47 Ω series; true & inverted
Clock output rate	100 MHz maximum
Clock out delay	11 ns maximum in 9 steps
Clock input type	TTL – 10H124
Clock input rate	dc to 100 MHz
Pattern input type	TTL – 10H124 (no connect is logic 1)
Clock-in to clock-out	approximately 30 ns
Pattern-in to recognition	approx. 15 ns + 1 clk period
Recommended lead set	HP 10474A



10463A ECL CLOCK POD

Clock output type	10H116 differential unterminated; and differential with 330 Ω to –5.2V and 47 Ω series
Clock output rate	200 MHz maximum
Clock out delay	11 ns maximum in 9 steps
Clock input type	ECL – 10H116 with 50 KΩ to –5.2v
Clock input rate	dc to 200 MHz
Pattern input type	ECL – 10H116 with 50 KΩ no connect is logic 0)
Clock-in to clock-out	approximately 30 ns
Pattern-in to recognition	approx. 15 ns + 1 clk period
Recommended lead set	HP 10474A



HP 1660C/CS/CP-Series Ordering Information

HP 1660C/CS/CP Series Benchtop Logic Analyzers

HP 1660C	136-Channel 100-MHz State/500-MHz Timing
HP 1660CS	136-Channel 100-MHz State/500-MHz Timing with Integrated 2-Channel 1-GSa/s Oscilloscope
HP 1660CP	136-Channel 100-MHz State/500-MHz Timing with Integrated 32-Channel 200M Vectors /sec Pattern Generator and Ethernet LAN[13]
HP 1661C	102-Channel 100-MHz State/500-MHz Timing
HP 1661CS	102-Channel 100-MHz State/500-MHz Timing with Integrated 2-Channel 1-GSa/s Oscilloscope
HP 1661CP	102-Channel 100-MHz State/500-MHz Timing with Integrated 32-Channel 200M Vectors /sec Pattern Generator and Ethernet LAN[13]
HP 1662C	68-Channel 100-MHz State/500-MHz Timing
HP 1662CS	68-Channel 100-MHz State/500-MHz Timing with Integrated 2-Channel 1-GSa/s Oscilloscope
HP 1662CP	68-Channel 100-MHz State/500-MHz Timing with Integrated 32-Channel 200M Vectors /sec Pattern Generator and Ethernet LAN[13]
HP 1663C	34-Channel 100-MHz State/500-MHz Timing
HP 1663CS	34-Channel 100-MHz State/500-MHz Timing with Integrated 2-Channel 1-GSa/s Oscilloscope
HP 1663CP	34-Channel 100-MHz State/500-MHz Timing with Integrated 32-Channel 200M Vectors /sec Pattern Generator and Ethernet LAN[13]
HP 1664A	34-Channel 50-MHz State/500-MHz Timing

Logic Analyzer Probes

Every HP 1660-Series logic analyzer ships standard with a complete probe kit that contains all of the acquisition cables (p/n 01660-61605), lead sets (01650-61608), grabbers (5090-4356) and other accessories that you require for general purpose logic analysis. The HP 1660CP-Series requires the appropriate clock and data pods to be ordered as options as noted below.

Additional HP 1660C/CS/CP Series Product Options

Option 015	Ethernet LAN interface [13]
Option 0B1	Extra User Manual
Option OB3	Add Service Manual
Option OBF	Add Programming Manual
Option 908	Rack Mount Kit
Option UK9	Front Panel Cover
Option W30	3-Year extended repair service
Option W50	5-Year extended repair service

HP 1660CP Series Required Product Options

Option 011	TTL Clock Pod and Lead Set (1 ea 10460A + 1 ea 10474A)
Option 012	3-state TTL/3.3V Data Pod and Lead Set (1 ea 10466A + 1 ea 10474A)
Option 013	3-state TTL/CMOS Data Pod and Lead Set (1 ea 10462A + 1 ea 10474A)
Option 014	TTL Data Pod and Lead Set (1 ea 10461A + 1 ea 10474A)
Option 021	ECL Clock Pod and Lead Set (1 ea 10463A + 1 ea 10474A)
Option 022	ECL (terminated) Data Pod and Lead Set (1 ea 10464A + 1 ea 10474A)
Option 023	ECL (unterminated) Data Pod and Lead Set (1 ea 10465A + 1 ea 10347A)

Note: For the pattern generator of HP 1660CP-series, please order at least one clock pod and at least one data pod for every eight (8) output channels from the above options or accessories listed on page 12.

HP 1660C/CS/CP Series Upgrades

HP E2460CS [12]	Upgrade to add two-channel 1-GSa/s, 250-MHz BW oscilloscope to any of the HP 1660CS series (oscilloscope upgrade does not apply to HP 1660A-series)
HP E2495A [12]	Upgrade to add 32-channel, 200 M Vectors/sec pattern generator (this upgrade does not apply to the HP 1660CS-series and HP 1664A)
HP E2427B	Add keyboard with DIN connector (PC style)
HP E2427A	Add keyboard with HIL connector (HP 1664A only)
HP E2472A [12]	Upgrade to add LAN capability to HP 1660C/CS series (this upgrade does not apply to the HP 1664A)
HP E2460B† [12]	Upgrades HP 1661C/CS to 136-channel HP 1660C/CS model, option 001 upgrades channel count of HP 1662C/CS to 1660C/CS, option 002 upgrades channel count of HP 1663C/CS to 1660C/CS
HP E2461B† [12]	Upgrades HP 1662C/CS to 102-channel 1661C/CS model, option 001 upgrades channel count of 1663C/CS to 1661C/CS
HP E2462B† [12]	Upgrades HP 1663C/CS to 64-channel 1662C/CS model
HP E2469A [12]	Upgrade HP 1660A/AS series to HP 1660C/CS series (includes LAN capability—do not order additional HP E2472A)

Accessory Software

HP B3740A	Software Analyzer
Opt AJ4	IBM, 3.5" Media/Documentation
Opt AAY	HP 9000 Series 700 Media/Documentation
Opt AAV	SUN (Solaris and SUN OS) Media/Documentation
Opt UDY	IBM Single User License
Opt UBY	HP 9000 Series 700 Single User License
Opt UBK	SUN (Solaris and SUN 0S) Single User License
HP 10391B	Inverse Assembler Development Package

[12] Upgrade includes cost of installation at a Hewlett-Packard Service Center. Upgrade is not customer installable.

[13] Ethernet LAN interface is included standard on the HP 1660CP-series and HP 1670D-series models. LAN is optional on the HP 1660C-series and HP 1660CS-series. LAN is not available on the HP 1664A.

† Channel count upgrades do not apply to the HP 1664A.

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Additional Ordering Information

State/Timing Analyzer Probes & Lead Sets

HP 5959-9333	Five grey probe leads for HP 1660X-Series
HP 5959-9334	Five short ground leads for HP 1660X-Series
HP 5959-9335	Five long ground leads for all state and timing
HP 01650-61608	16-Channel probe lead set for state and timing analyzers
HP 01650-63203	Termination adaptor for state and timing analyzers
HP 1810-1278	9-Channel IC termination (DIP)
HP 1810-1588	Termination IC SIP
HP 1251-8106	2 × 10, 0. 1-inch center header (Similar to 3M p/n 2520-6002)
HP 5090-4356	Surface-mount grabbers (package of 20)
HP 5959-0288	Throughhole grabbers (package of 20)

Other Accessories for HP Logic Analyzers

HP 1180B	Testmobile for HP 1660-series
HP 92199B	Power strip
HP 5041-9456	Front cover for HP 1660-series
HP 5062-7379	Rack mount kit for HP 1660 Series

Oscilloscope Probes and Accessories [1]

HP 10433A	10:1, 10 MΩ, 10 pF mini-probe, 2 m
HP 10437A	1:1, 50 Ω mini-probe, 2 m
HP 10439A	1:1, 1 MΩ, 64 pF mini-probe, 2 m
HP 10440A	100:1, 10 MΩ 2.5 pF mini-probe, 2 m
HP 10441A	10:1, 10 MΩ, 9 pF mini-probe, 2 m
HP 1145A	Dual 10:1, 1.6pF, 1 MΩ active probe

Pattern Generator Accessories

HP 10460A	TTL Clock Pod for the HP 1660CP-series
HP 10461A	8-channel TTL Data Pod for the HP 1660CP-series
HP 10462A	8-channel 3-state TTL/CMOS Data Pod for the HP 1660CP-series
HP 10463A	ECL Clock Pod for the HP 1660CP-series
HP 10464A	8-channel ECL (terminated) Data Pod for the HP 1660CP-series
HP 10465A	8-channel ECL (unterminated) Data Pod for the HP 1660CP-series (use HP 10347A lead set)
HP 10466A	8-channel 3-state TTL/3.3V Data Pod for the HP 1660CP-series
HP 10474A	8-channel Probe Lead Set for the HP 1660CP-series
HP 10347A	8-channel (50-ohm Coaxial) Probe Lead Set

Related HP Literature

Title	Publication Description	HP Pub. Number
HP 1660C/CS-Series and HP 1670D-Series Logic Analyzers	Color Brochure	5964-3665E
The HP 1660CP-Series Logic Analyzers With Integrated 32-Channel 200 mVectors/Sec Pattern Generator	Color Photo Card	5966-1490E
The HP 1670-Series Benchtop Logic Analyzers	Technical Specifications	5964-3666E
Introduction to the HP 1660C/CS and 1670D-Series Logic Analyzers	Video (NTSC) Video (PAL)	5965-7501EUS 5965-7501E

Warranty Information

All Hewlett-Packard products described in this document are warranted against defects in material and workmanship for a period of one year from date of shipment. Option W03 provides a three-month on-site warranty in lieu of the standard one-year return-to-HP warranty. Three-year and five-year return-to-HP repair services are also available. Refer to individual product manuals for detailed descriptions and terms of warranty.

[1] Please refer to HP 1664A Product Specifications and Characteristics on page 9.

For more information about Hewlett-Packard test & measurement products, applications, services, and for a current sales office listing, visit our web sites:
http://www.hp.com/go/tmdir
http://www.hp.com/go/logicanalyzer
http://www.hp.com/go/emulator
You can also contact one of the following centers and ask for a test and measurement sales representative.

United States:
Hewlett-Packard Company
Test and Measurement Call Center
P.O. Box 4026
Englewood, CO 80155-4026
1 800 452 4844

Canada:
Hewlett-Packard Canada Ltd.
5150 Spectrum Way
Mississauga, Ontario
L4W 5G1
(905) 206 4725

Europe:
Hewlett-Packard
European Marketing Centre
P.O. Box 999
1180 AZ Amstelveen
The Netherlands
(31 20) 547 9900

Japan:
Hewlett-Packard Japan Ltd.
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